Model 66 ADC
A/D CONVERTER

DESCRIPTION

The RFL Model 66 ADC is one of the Series 66 TDMS plug-in modules. Its purpose is to convert an analog voltage to a binary or BCD digital number. The conversion technique used is offset, dual-slope integration which gives a high degree of accuracy and noise rejection without the need for filters. A choice of crystals is provided to obtain optimum noise rejection. The choice depends upon whether the output is binary or BCD and whether the local power source is 50 Hz or 60 Hz. The unit also features differential inputs and adjustable settling time.

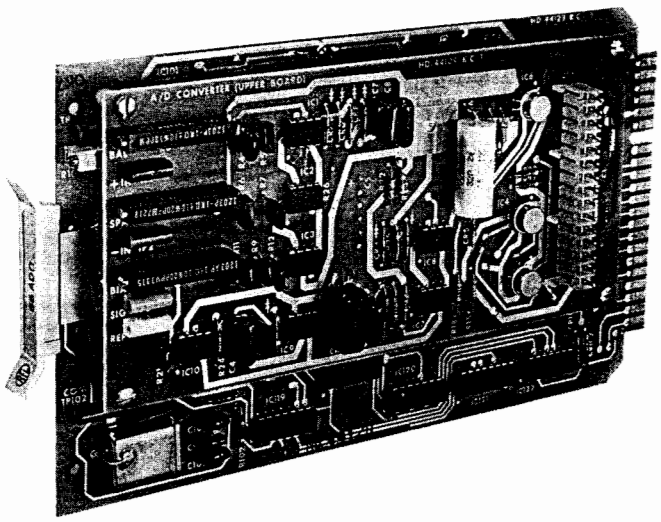


Figure 1. Model 66 ADC A/D Converter.

SPECIFICATIONS

Input Range: −1.999 to +1.999 Vdc for BCD outputs
−2.047 to +2.047 Vdc for binary outputs
±1 V common mode

Input Circuit: Differential inputs
Input impedance > 1 megohm
Input bias current $< 0.25\ \mu A$

Digital Outputs: 12 bits BCD or 10 bits binary,
1 bit overrange,
1 bit sign and
1 bit overflow.

15 bits total BCD
13 bits total binary.

Accuracy: ±2 mV at 25°C
±5 mV from the 25°C reading over 20°C to +70°C range
±6 mV from the 25°C reading over 30°C to +75°C range

Conversion Time: Settling time +40 mS max. for 60 Hz rej.
Settling time +48 mS max. for 50 Hz rej.

Adjustments: Balance (Common mode rejection)
Span
Bias
Settling Time

Power: +(11 to 13) Vdc @ 35 mA
−(11 to 13) Vdc @ 20 mA

Size: Three standard one-half-inch module increments in RFL Model 68 Chassis.

ORDERING INFORMATION

When ordering, the crystal frequency option must be specified. Refer to Tables 1 and 2 to determine which option is suitable.

TABLE 1

Module Designation	A/D CONVERTER CARD					
	HB-44120	HB-44116-1 Option Xtal for BCD - 60 Hz	HB-44116-2 Option Xtal for Binary - 60 Hz	HB-44116-3 Option Xtal for BCD - 50 Hz	HB-44116-4 Option Xtal for Binary - 50 Hz	
66 ADC-1	•	•				
66 ADC-2	•		•			
66 ADC 3	•			•		
66 ADC-4	•				•	

TABLE 2

CRYSTAL FREQUENCY OPTIONS			
Option P/N	Crystal Frequency	Output Type	Local Power Line Frequency
HB-44116-1	3.84000 MHz	BCD	60 Hz
HB-44116-2	3.93216 MHz	Binary	60 Hz
HB-44116-3	3.20000 MHz	BCD	50 Hz
HB-44116-4	3.27680 MHz	Binary	50 Hz

CONNECTIONS

The least significant ten binary or 12 BCD bits are available at the terminals indicated on the schematic Figure 6. OVERRANGE at Terminal Y is the most significant bit; it represents 2^{10} for binary and 1000 for BCD conversions. The polarity information is available at the SIGN Terminal L; this bit will be high for negative input voltages, and low for positive inputs. The OVERFLOW signal at Terminal Z will be high if the input signal exceeds the specified input range.

The system designer should keep in mind that all of the output signals mentioned so far will be subject to changing status during the conversion process. It is also worth noting there is never an ambiguous zero state. Zero volts at the input will always have a positive polarity.

The BIN/BCD Terminal K controls whether the conversion will be binary or BCD. This input should be wired to +V for binary or to Com for BCD. Whenever the type of conversion is changed, the unit must be recalibrated.

A positive going transition at START A/D Terminal 22 will start the conversion process, and Terminal X, IN PROGRESS, will be low while the conversion is taking place. CHAN ADV CLOCK at Terminals 18 and V will drop to a logic zero at the start of conversion and remian low during the settling time period. CHAN ADV CLOCK may be wired directly to Terminal V of an Analog Multiplex Card, Model 66 AMUX, equipped with a Sequencer, Option HB-44129-10. Two typical schemes demonstrating the use of these terminals are shown in Figures 2a and 2b.

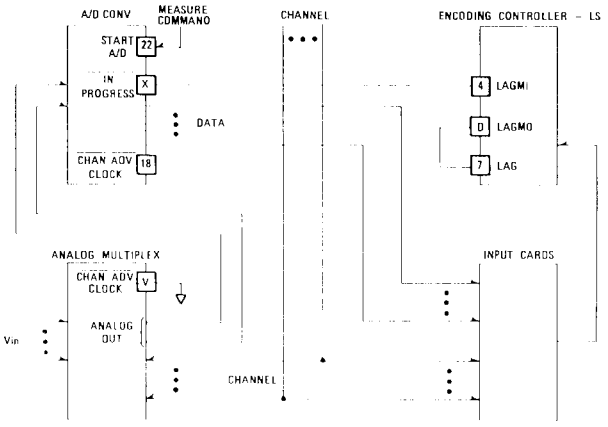


Figure 2(a). Example showing a system wired for an external-measurement command on an external-channel selection. After A/D conversion, the encoder sends one message.

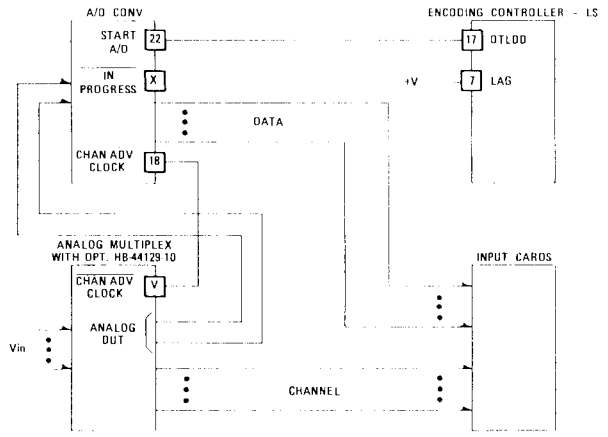


Figure 2(b). Example showing a system wired to send messages continuously and to sequence the multiplexer. Time to send message must be longer than the conversion time.

Inputs are connected to Terminal 6 (+) and Terminal 5 (–). It is important to have a dc return path from the voltage source being measured to Signal Common at Terminal 4. Figure 3 shows the preferred termination.

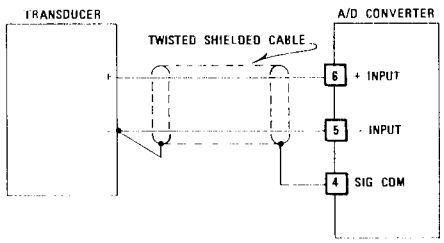


Figure 3. Recommended method for terminating input-signal connections.

ADJUSTMENTS

Settling time may be adjusted using R106 on the bottom board, and it may be monitored with a scope connected to TP101 (BLUE-HI) and TP102 (BLACK-LO). The scope should display a logic 1 level during settling. The purpose of settling time is to hold off the A/D conversion process until the input signal has stabilized.

In some applications, such as monitoring slowly changing levels where the A/D or Analog Multiplex Cards are always connected to the transducer, the signal is already stabilized, and the settling time can be set to minimum. In other applications the same command to start A/D conversion may also have been used to change the variable being measured, or it may have energized relays and required charging of filter networks. Settling time adjustment would then directly affect accuracy if it were set too short.

The BAL pot, R3, Figure 7, should be adjusted prior to setting the SPAN and BIAS controls, R8 and R10. The input signal to the card should be disconnected and a jumper installed between TP1 GREEN and TP2 GRAY.

Connect a 50-Hz or 60-Hz signal, 2 V p-p, from TP1 GREEN to TP4 WHITE. Adjust BAL until a scope connected to TP3 ORANGE HI and TP4 WHITE LO indicates minimum AC voltage on its screen. Disconnect jumper, AC signal source and scope. Reconnect input signal unless SPAN and BIAS are to be adjusted.

SPAN and BIAS settings are adjustable with potentiometers on the upper board. Their setting is a "trial and error" process. Connect a stable and adjustable voltage source across the input Terminals 5 = – and 6 = + of the basic board. Also short Terminal 4 to Terminal 5. The input level may be monitored at TP1 GREEN (+) and TP2 GRAY (–). Switch the input levels between 10% and 90% of scale and adjust SPAN and BIAS until the digital error is zero at those two points. Remove the voltage source and the short at Terminals 4 and 5; then reconnect the input signals.

THEORY OF OPERATION

The Model 66 ADC uses an offset, dual-slope integration technique to perform the analog-to-digital conversion. It can be shown that if an input signal is integrated for a known time period, then the time it takes the integrator to return to its starting point by integrating a known voltage is proportional to the input voltage. In formula form:

$$Tx = \frac{V_{in}\ T_{ref}}{V_{ref}}.$$

Because the unit must handle negative input voltages, the input voltage to the integrator is offset and the unknown time adjusted accordingly.

$$Tx + Tos = \frac{(V_{in} + V_{os})\ T_{ref}}{V_{ref}}.$$

Good noise rejection is inherent with this technique. If T_{ref} is made equal to the period of the power line, any stray pickup from the power lines will cancel in the integration process.

Figure 4 shows a block diagram of the A/D converter. The input signal is first amplified by –1.5 then fed into a scaling amplifier where it is mixed with a reference voltage to give an output equal to 1.5 V_{in} + 4.5 volts. The first Analog Switch is controlled by the Timing-and-Control Logic which will allow the offset input to be gated through the second Analog Switch to the integrator for one period of the power line and then gate through the –6-volt reference voltage. The Comparator determines the starting point and finishing point of the integration cycle. The second Diff Amp and second Analog Switch are used to keep the integrator in a ready position when conversion is not taking place. Timing periods in the unit are crystal-controlled and counted using an up/down counter. Parallel outputs from the up/down counter are used directly to provide the digitized value of the input voltage.

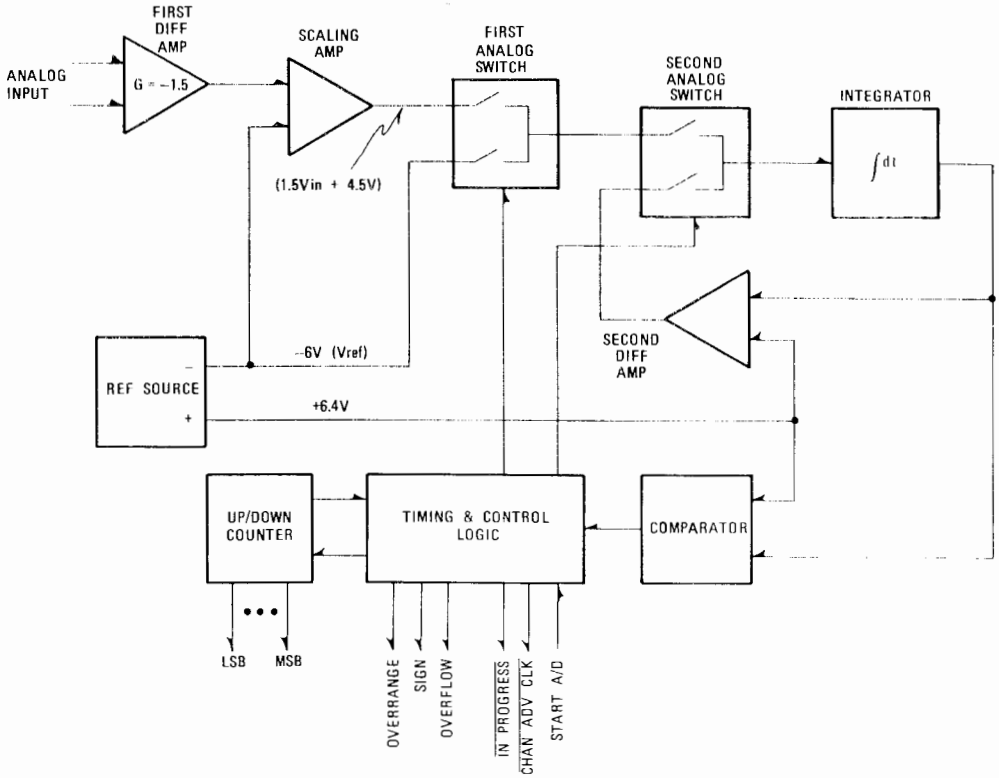


Figure 4. Block Diagram, A/D Converter.

To get more specific about the detailed circuitry of each block, the discussion will start with the Reference Source. The circuits about IC9 and IC10 at Zones (C3) and (B3) on the upper board Figure 7, form the reference circuit. A constant 4-mA current is maintained in zener CR1 by keeping 6 volts across R19. The voltage on the cathode of CR1 (B3) will be +6.4 volts; this voltage is inverted and scaled to −6 volts at the output of IC10. Thus the circuit provides +6.4 volts, −6 volts and its own regulated current source. Since this circuit has two stable states, R22, R23, CR2, and CR3 are used to assure the correct polarity during power turn on.

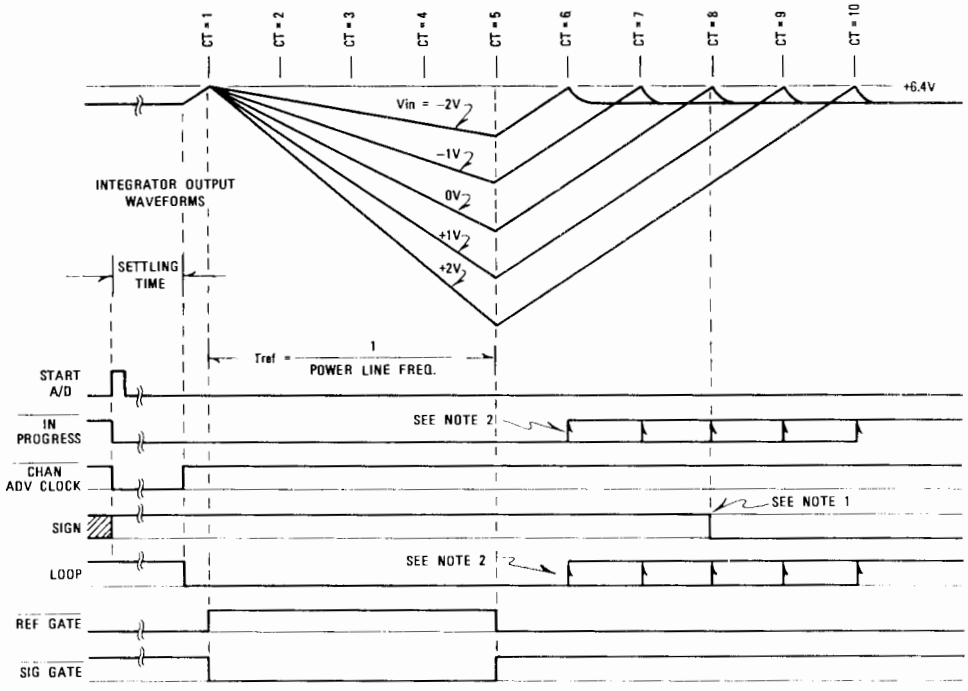
IC1 and IC2, (B2, C2) Figure 7 form the first Diff. Amp. It can be shown that the output of IC2 will equal −1.5 times the difference in voltage between Terminals J1-7 and J1-8. BAL pot, R3, (A2) is provided to compensate for any resistance errors due to normal tolerances in the string comprised of R4 through R7. CR6 through CR9 (B1, B2) act as protective clamps for surges at the input. Since both inputs are connected to the non-inverting terminals of operational amplifiers, the input impedance is extremely high. IC3 (D2) and its associated resistors offset the amplified input signal. As such, negative input voltages in the specified range will not cause the output of IC3 to be negative, and hence, integration of this signal will always be in just one direction. IC4 (E2) and IC5 (F2) are the analog switches; and IC6 (G2), along with R13 and C6, form the integrator.

When no A/D conversion is taking place, IC5-5 will be connected to IC5-4, and the output of the integrator will be fed back to its own input through the differential amplifier composed of IC7 (F3) and R15 thru R18. This circuit will stabilize when the voltage on the right side of R18 equals the voltage on the right side of R16 which is one diode drop below +6.4 volts.

Figure 5 shows a timing diagram and includes the integrator waveforms for various input signals. Until $\overline{\text{CHAN ADV CLOCK}}$ returns high, and after the A/D conversion when $\overline{\text{IN PROGRESS}}$ goes high, the LOOP signal will keep the integrator fed back on itself through IC7, as described in the previous paragraph.

After the settling time, a −6 volt reference is switched to the integrator through IC4-4 because the $\overline{\text{REF GATE}}$ is low. When the integrator output hits +6.4V, as detected by IC8 (G2) which is used as a comparator, the control logic switches $\overline{\text{REF GATE}}$ high and $\overline{\text{SIG GATE}}$ low to connect IC4-8 to IC4-9 and, thus, the ($1.5V_{in}$ +4.5) signal is routed into the integrator. This condition is maintained for exactly the period of the power line voltage. Next the reference voltage is redirected to the integrator. The time it takes for the integrator to return to +6.4V, once again detected by IC8, is directly proportional to the output of IC3. When IC8-6 goes high, signifying +6.4V has been hit, the loop IC6 to IC7 to IC5 to IC6 is re-closed. The A/D will now wait for the next START A/D command. This completes the details of the upper board.

The Timing and Control Logic and the up/down counter circuits are located on the lower printed circuit board, shown schmetically in Figure 6. IC101, IC102, and IC103 are used for up/down counting. Their outputs are buffered



NOTE 1. SIGN STAYS HIGH IF INTEGRATOR HITS +6.4V BEFORE CT = 8, OTHERWISE IT WILL DROP TO LOGIC ZERO.

NOTE 2. THESE WAVEFORMS GO POSITIVE WHEN INTEGRATOR HITS +6.4V.

Figure 5. Timing Diagram, Model 66 ADC.

by IC114 and IC110 (C1 thru G1) and then made available at the card-edge terminals as the least significant bits.

To understand the lower board, the discussion will begin with START A/D at Terminal 22, Figure 6, (B5). A positive going transition from 0 to 1 will set IC122A which in turn will force IC120D-11 low. Because IC120C-9 was low, IC120C-10 will go high and set IC117A (C4). At the same time, the output of IC113D (C5) drops to zero for the IN PROGRESS signal. IC117A (C4) is used to trigger the settling-time pulse generator IC106 (D4). While the output of IC106 is high, all of the other logic on the board is initialized.

The pulse width generated by IC106 is approximately 1.1 RC where R is R105 in series with R106, and C is C104. Thus the maximum settling time is about 110 mS. For some applications this time will need to be increased. Enlarging the value of C104 is the preferred method.

After the settling time, both inputs to IC118A (B3) will be low and the integrator will not be looped back on itself. The REF GATE signal at IC118C-10 (A4) will be low, thus gating the reference signal to the integrator. Eventually the integrator will hit +6.4 volts and Interboard Post 11 (A4) will go high. IC113A and IC113B (A4) are wired with R103 and R104 to provide a snap-action to the comparator's output.

IC117B (E3) was triggered by IC113A (A4) thus enabling the counting circuits. Also, the logic 1 was removed from IC118C (A4) to permit integration of the signal. The signal will continue to be integrated until IC111-1 (C4) goes high or CT = 5.

At this time it will be worth a few paragraphs to discuss the significance of the CT = signals and the up/down-count philosophy.

No matter whether the counters IC101, IC102, and IC103 are counting up or down, it takes an equal amount of time for the outputs to change by 1 bit. Likewise it takes the same time going either direction to count from a 000 state to a 000 state. Each time the 000 state occurs IC111 will be incremented by one count. Initially the three IC's will be counting down. When CT = 8 first occurs, the down sequence will change to an up sequence; however, the time between increments of IC111 will remain equal.

The reason for counting down, then counting up, is to make the digital outputs correspond to the way people think of positive and negative numbers: −9, −8, . . . −1, 0, +1, . . . +8.

In Figure 5, the timing diagram, it can be seen that from CT = 1 to CT = 5 the signal is being integrated. The crystal frequencies were selected to make the time between each CT equal to a fourth of the power line period. Also note that the input voltage determines in which CT interval the integrator output hits +6.4 V. A zero-volt input will cause the end of integration at exactly the beginning of CT = 8, which is when the up-count sequence begins.

The following things can also be seen from Figure 5. The output SIGN will be high during down counting. If CT = 5, or if CT = 6 and the counters are in the 000 state or if CT = 10, then OVERFLOW will be true. If CT = 6, or if CT = 7 and the counters are in the 000 state, or if CT = 9, then OVERRANGE (which is really the most significant bit) will be true.

Referring to some of the circuitry, IC111 (C4) will be incremented by a positive going transition at Pin 14. This means all the inputs to IC107A (D3) must be low. IC107A−3, −4, −5 come from other gates which detect when the counters are all zeros. IC107A−2 is the common clock line, which was included to prevent erroneous updating of IC111 due to "slivers" in the logic circuits. During initialization the common clock coming from IC115B (B3) is high and IC111 is in the 0 state (which is also the CT = 10 state). When the first clock pulse comes through, IC111 is incremented immediately. That is why the timing diagram starts at CT = 1 instead of CT = 0. (In other words, CT = 0 lasts for only ½ a clock pulse).

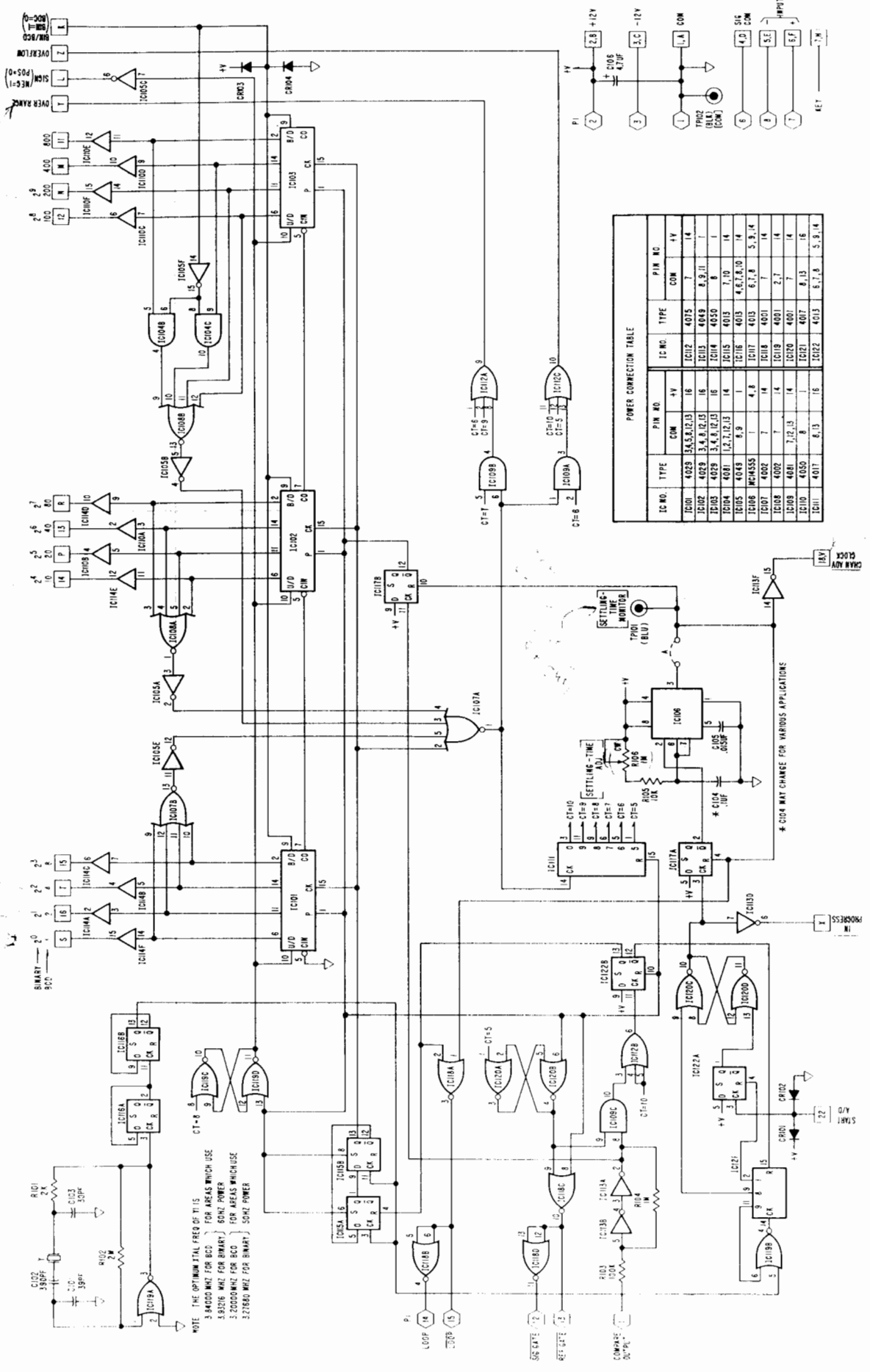
As was stated previously, the signal is integrated until CT = 5. When CT = 5, IC120A (B3) and IC120B (B4), which are wired together as a set-reset flip-flop, are set, and IC120B-4 goes high. This causes the output of IC118C (A4) to drop and allow reference integration. It also enables IC122B (C4) to be set if the proper conditions exist. More will be said about IC122B later.

Up and down counting by IC101, IC102, and IC103 and SIGN through IC105C (H1) are controlled by the set-reset flip-flop made up of IC119C and IC119D (B2). Initially the flip-flop is reset during settling, but at CT = 8 it is set. OVERFLOW comes from IC112C (F4), and OVERRANGE comes from IC112A (F3). Both IC's are OR gates; their inputs were described earlier by looking at the timing diagram.

IC122B (C4) can be set by either of two conditions, the first occurs when the comparator senses the integrator hit +6.4 volts, as at the end of conversion, or secondly an overflow condition is detected (CT = 10) by the presence of a large positive input signal. Setting of IC122B is the beginning of the end. IC115A (A3) is reset, and after the next clock pulse to IC115B−11 (B3), the common clock line originating at IC115B-13 will drop low and stay low. Also the reset signal is removed from IC121 (A5). IC121 gets IC122A (B5) ready to accept the next start pulse, and it provides a short delay before the IN PROGRESS signal is raised.

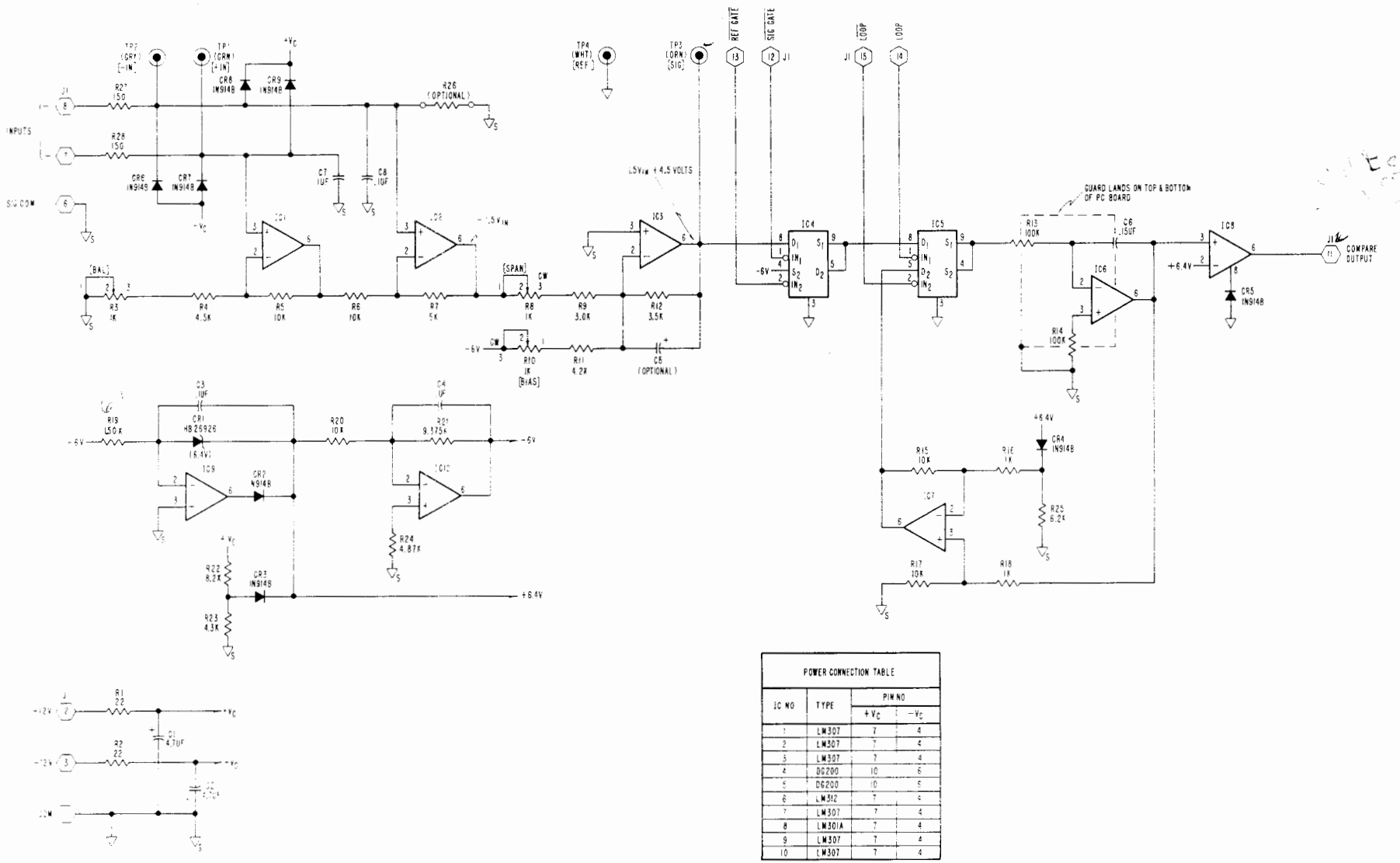
Table of Replaceable Parts

DIAGRAM SYMBOL	NAME OF PART AND DESCRIPTION	RFL PART NO.
C1, 2	Capacitor, tantalum, 4.7 μF, 20%, 20 V, Kemet T324B475M020AS, or eq.	H-1007-711
C3, 4, 7, 8	Capacitor, met., poly. 0.1 μF, 10%, 250 V, Seacor 106-0.1, or eq.	H-1007-1255
C5	Capacitor, option, value as required by sales order	
C6	Capacitor, poly., 0.15 μF, 2%, 100 V, Wesco 32P, or eq.	H-5115-89
C101	Capacitor, mica, 39 pF, 5%, 100 V, Electromotive DM-10, or eq.	H-1080-385
C102	Capacitor, mica, 390 pF, 5%, 100 V, Electromotive DM-10, or eq.	H-1080-379
C103	Capacitor, mica, 30 pF, 5%, 100 V, Electromotive DM-10, or eq.	H-1080-391
C104	Capacitor, ceramic, 0.1 μF, 10%, 50 V, Type CK05, according to RFL Spec HA-38309	H-0100-3
C105	Capacitor, ceramic, 0.015 μF, 10%, 50 V, Type CK05, according to RFL Spec HA-38309	H0100-16
C106	Capacitor, tantalum, 4.7 μF, 20%, 20 V, Kemet T324B475M020AS, or eq.	H-1007-711
CR1	Zener diode assembly, 6.4 V, ±5%	HB-26926
CR 2-9, 101-104	Diode, Type 914B	HA-26482
IC1, 2, 3, 7, 9, 10	Operational amplifier, National LM307N, or eq.	H-0620-93
IC4, 5	Dual analog gate, Siliconix DG200BA, or eq.	H-0605-3
IC6	Operational amplifier, National LM312H, or eq.	H-0620-113
IC8	Operational amplifier, National 301AN, or eq.	H-0620-76
IC101, 102, 103	Presettable up/down counter, RCA CD4029AE, or eq.	H-0615-17
IC104, 109	Quad, 2-input AND gate, RCA CD4081BE, or eq.	H-0615-31
IC105, 113	Hex buffer/converter, RCA CD4049AE, or eq.	H-0615-7
IC106	Timer, National LM555CN, or eq.	H-0620-108
IC107, 108	Dual, 4-input NOR gate, RCA CD4002AE, or eq.	H-0615-16
IC110, 114	Hex buffer/converter, RCA CD4050AE, or eq.	
IC111, 121	Decade counter/divider, RCA CD4017AE, or eq.	H-0615-38
IC112	Triple, 3-input, OR gate, RCA CD4075BE, or eq.	H-0615-33
IC115, 116, 117, 122	Dual D flip-flop, RCA CD4013AE, or eq.	H-0615-1
IC118, 120	Quad, 2-input, NOR gate, RCA CD4001AE, or eq.	H-0615-30
IC119	Quad, 2-input NOR gate, Fairchild F4001 PC only	H-0615-64
R1,2,22,23,25,27,28, 101 thru 105	Resistor, fixed, composition, ¼ W, 5%, Allen Bradley CB, or eq. Value as shown on schematic	H-1009-XXX
R3, 8, 10	Potentiometer, metalized film, 1K, 10%, ½ W, Vishay 1203-P-1K, or eq.	HA-37423
R4, 5, 6, 7, 9, 11, 12, 20, 21	Resistor, metal-film, precisoin, 0.1%, 0.3W, 10 ppm/°C, 0.005%/yr Resnet Series 500, or eq. Value according to schematic	H-1510-XXX
R13-19, 26	Resistor, metal film, precision 1.0%, 1/8 W, Type RN550D, according to RFL Spec HA-38301. Value as shown on schematic. (Value of R26 is set by purchase specification)	H-1510-XXX
R106	Resistor, metal-film, variable 1000K, 0.75%, Helipot 79PR1M, or eq.	HA-40694
Y1	Crystal, piezoelectric, 3.84 MHz, Option HB-44116-1	HA-37440-52
Y1	Crystal, piezoelectric, 3.93216 MHz, Option HB-44116-2	HA-37440-53
Y1	Crystal, piezoelectric, 3.20 MHz, Option HB-44116-3	HA-37440-50
Y1	Crystal, piezoelectric, 3.27680 MHz, Option HB-44116-4	HA-37440-5
	Schematic (2 sheets)	HE-44122-



POWER CONNECTION TABLE								
IC NO.	TYPE	PIN NO.		IC NO.	TYPE	PIN NO.	
		COM	+V			COM	+V
IC101	4029	3,4,5,9,12,13	16	IC112	4075	7	14
IC102	4029	3,4,5,9,12,13	16	IC113	4049	8,9,11	1
IC103	4029	3,4,5,9,12,13	16	IC114	4050	8	1
IC104	4081	1,2,7,12,13	14	IC115	4013	7,10	14
IC105	4049	8,9	1	IC116	4013	4,6,7,8,10	14
IC106	MC4555	1	4,8	IC117	4013	6,7,8	5,9,14
IC107	4002	7	14	IC118	4001	7	14
IC108	4002	7	14	IC119	4001	2,7	14
IC109	4081	7,12,13	14	IC120	4001	7	14
IC110	4050	8	1	IC121	4017	8,13	16
IC111	4017	8,13	16	IC122	4013	6,7,8	5,9,14

Figure 6. Schematic of lower board, Model 66 ADC



POWER CONNECTION TABLE			
IC NO	TYPE	PIN NO	
		+Vc	-Vc
1	LM307	7	4
2	LM307	7	4
3	LM307	7	4
4	DG200	10	6
5	DG200	10	5
6	LM312	7	4
7	LM307	7	4
8	LM301A	7	4
9	LM307	7	4
10	LM307	7	4

Figure 7. Schematic of upper board, Model 66 ADC.